EE 211 Lecture 5

T. H. Ortmeyer

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This week’s labs

- Aliasing and Pulse Measurements
- 555 Timers
- Important Note: Next weeks schedule

Comments on WA#2

- Tables were much improved
- Those who didn’t get all three data points– what do you do?
- Discussion point– don’t just talk about the error
- Relate back to the predictive equation
- Lead resistance is a stretch in this case

Sampling Theorem

To ensure accuracy of sampled signals,

$f_s > 2\,f_{highest}$

where

f_s is the sampling rate of the digitizer

$f_{highest}$ is the highest frequency component of the sampled signal

$$f_{nyquist} = \frac{1}{2} f_{sampling}$$

Aliasing

If the sampling theorem is violated, aliasing occurs—

An illustrated on the web site

http://www.dsptutor.freeuk.com/aliasing/AD102.html

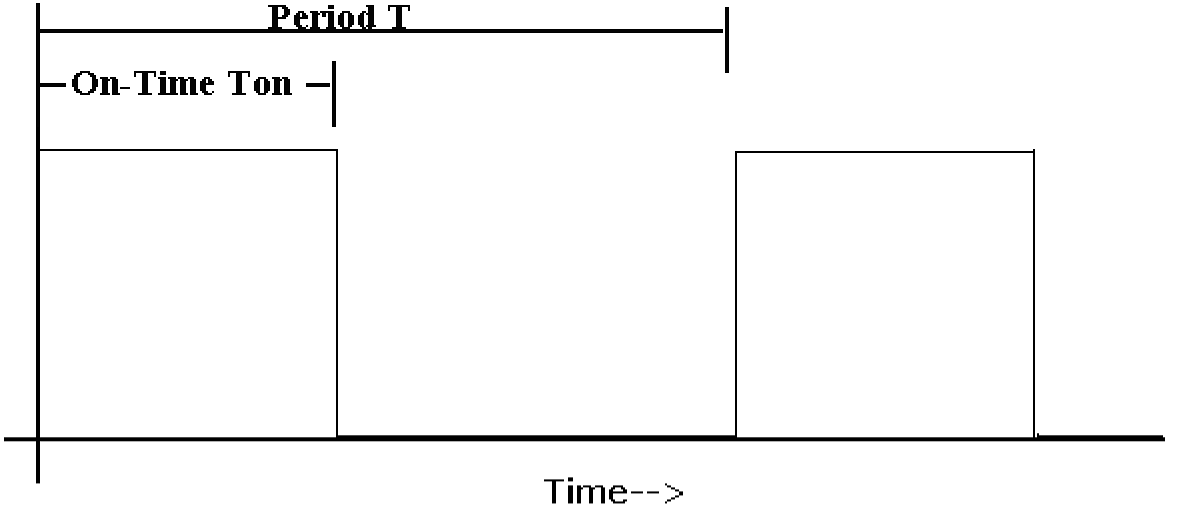
Labview "canned" programs

- Acquire Waveform.vi
  - Investigate aliasing

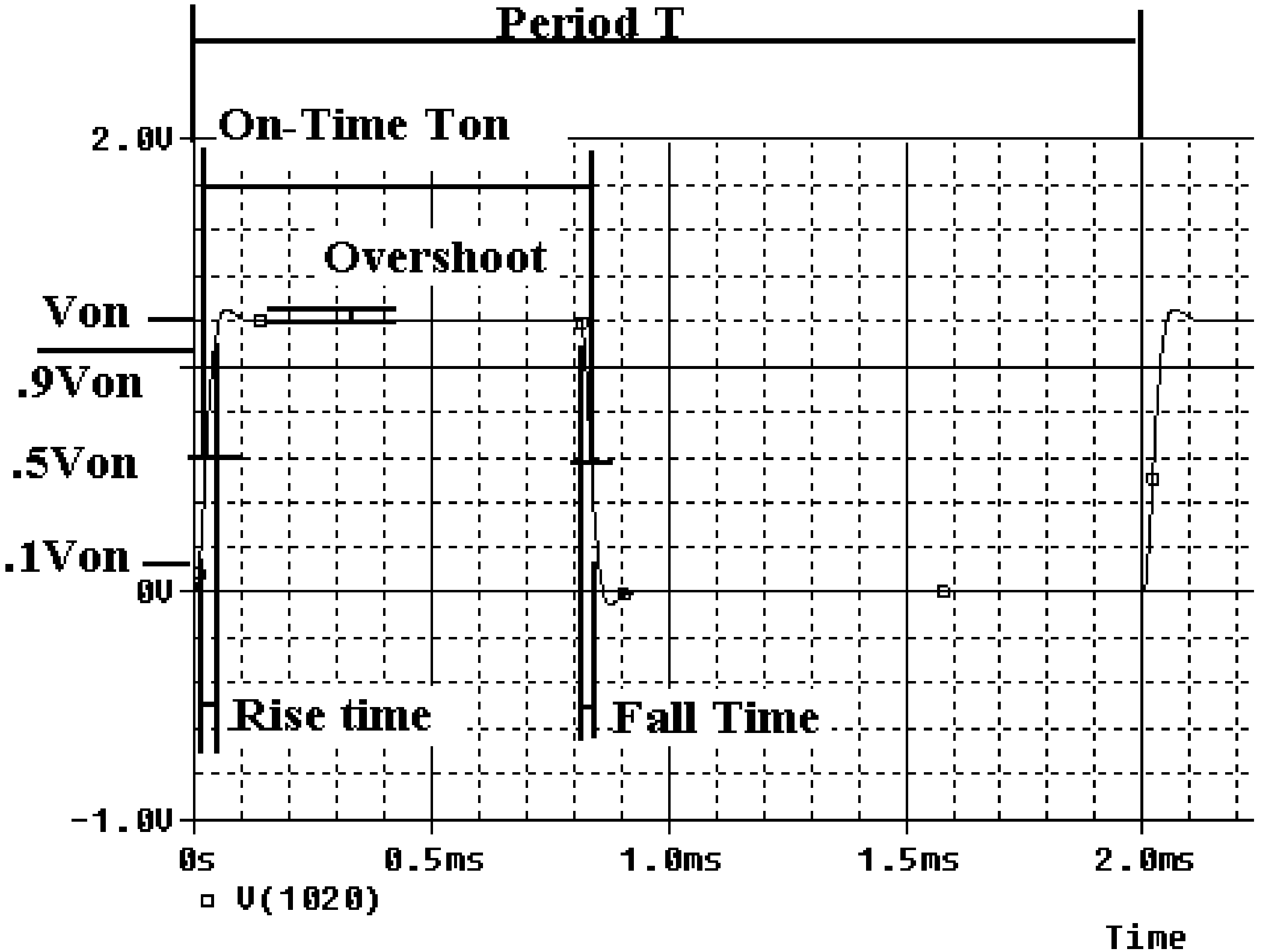
Pulse waveform qualities

- Amplitude
- Maximum
- Rise time
- Fall time
- Pulse width

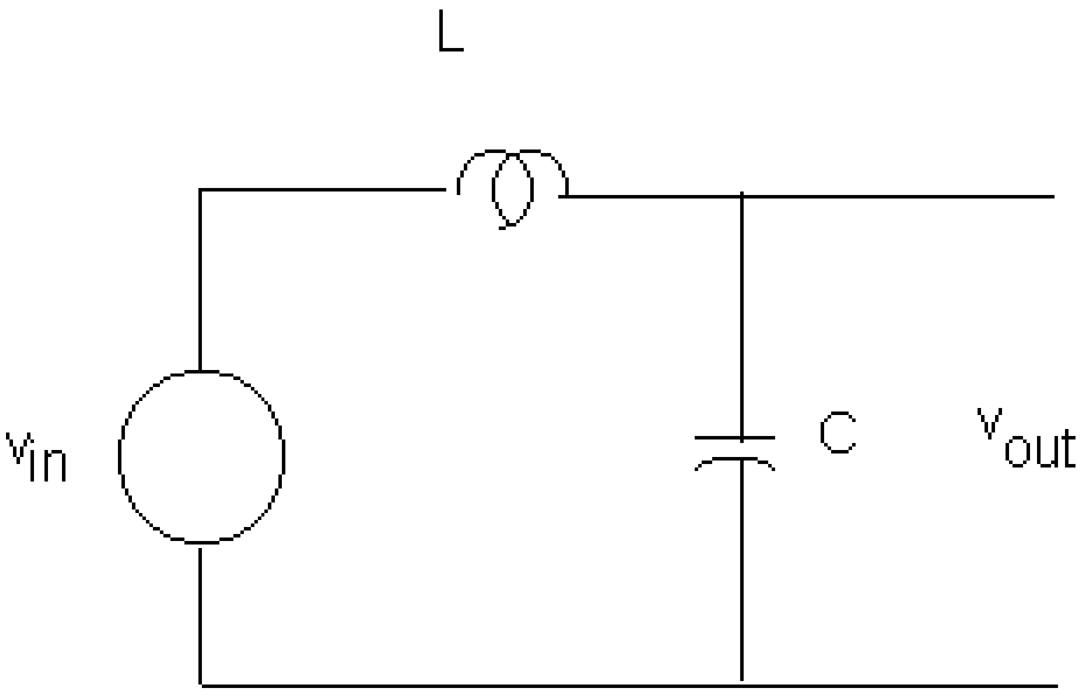
The ideal pulse train



The actual pulse train



Most circuits



Response to a step input

$$v_o(t) = V_i u(t)\left[1 - e^{-\alpha t}\cos\omega_d t\right]$$

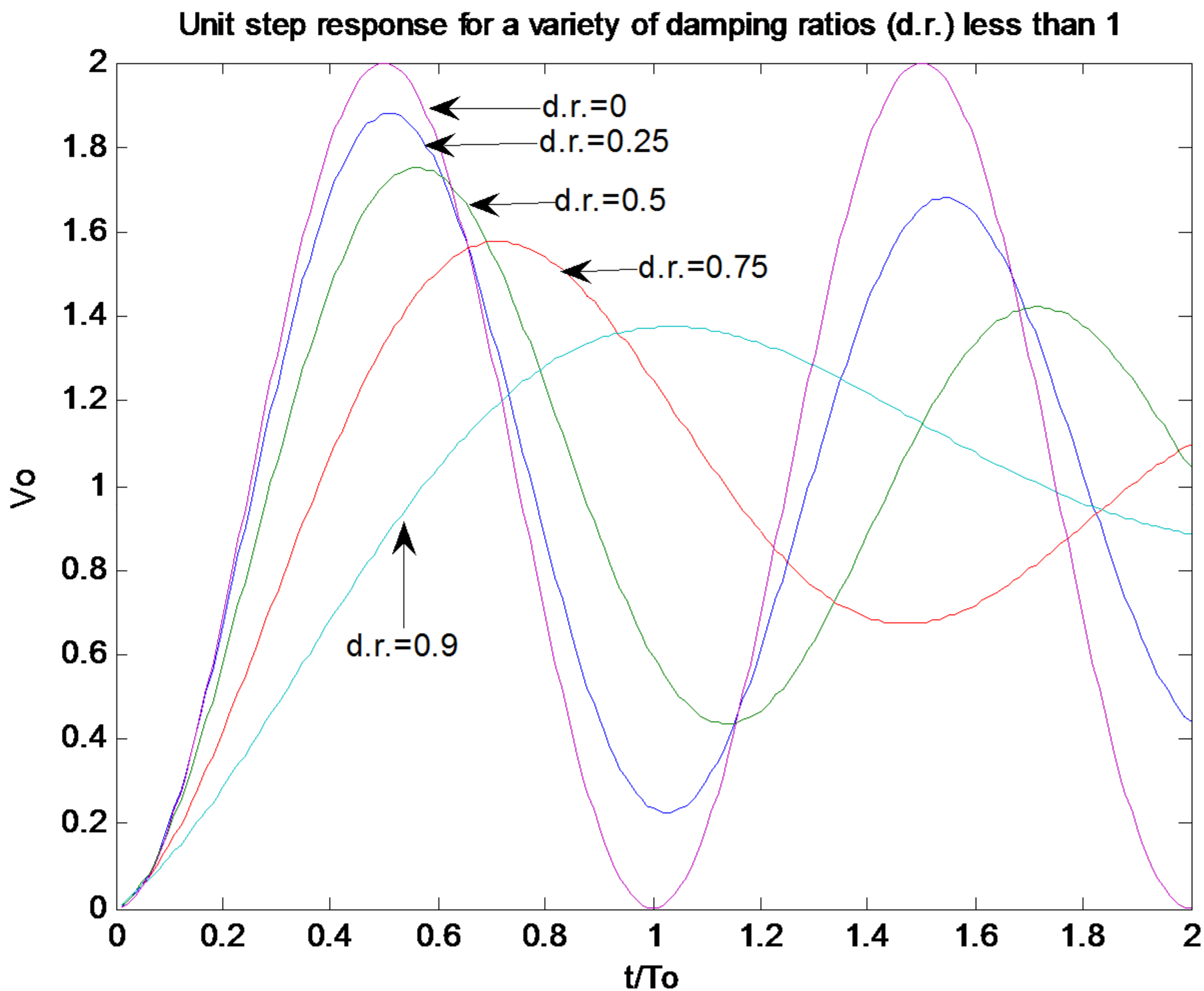
where

$$\omega_d = \sqrt{\omega_o^2 - \alpha^2} = \text{damped frequency}$$

$$\omega_\text{o} = \sqrt{\frac{1}{LC}} = \text{natural frequency}$$

$$\alpha = \frac{1}{2\text{RC}} = \zeta\omega_n$$

$$\zeta = \text{damping ratio}$$

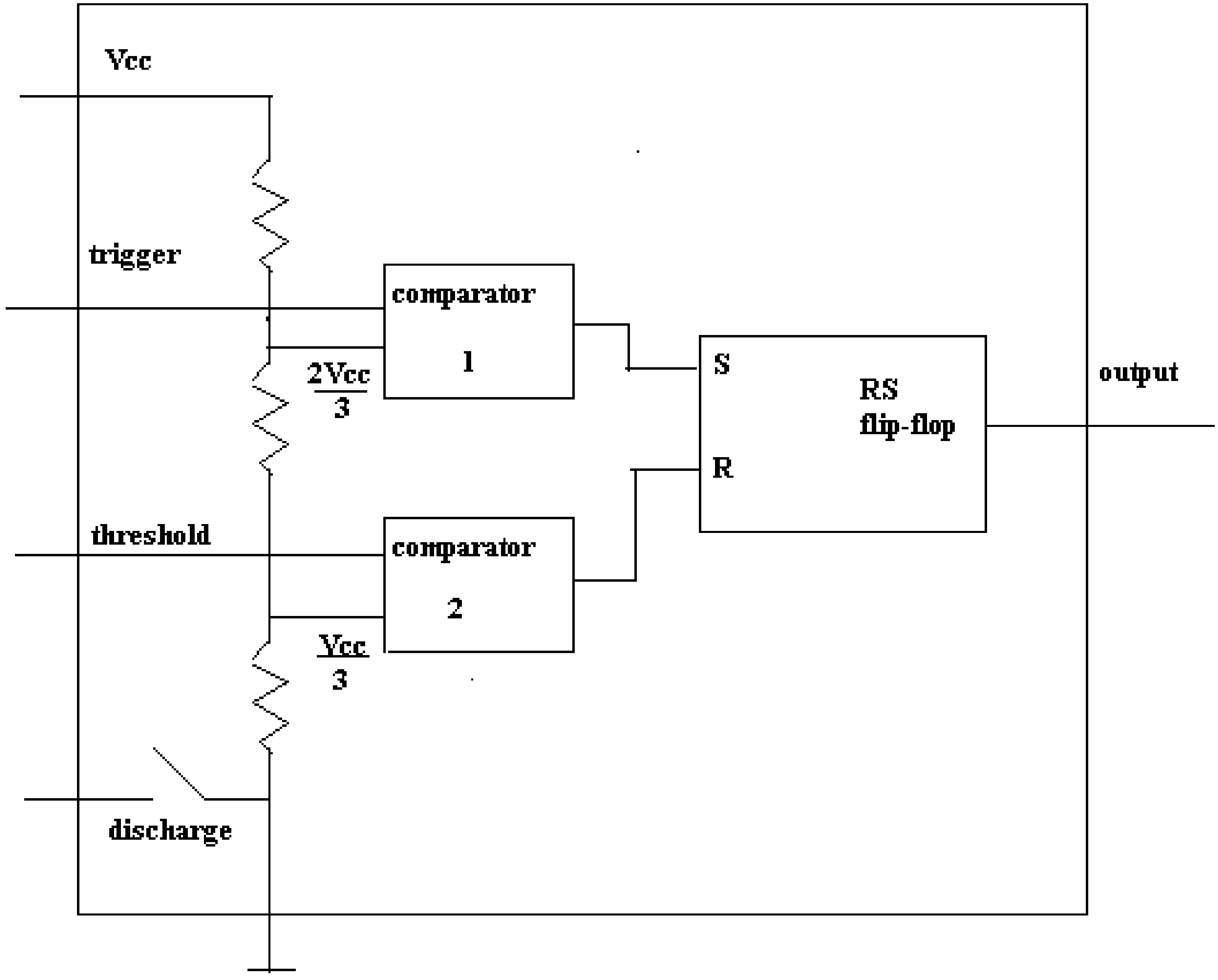

Unit step response for a variety of damping ratios (d.r.) less than 1
d.r.=0
d.r.=0.25
d.r.=0.5
d.r.=0.75
d.r.=0.9
Vo
t/To
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

Goal

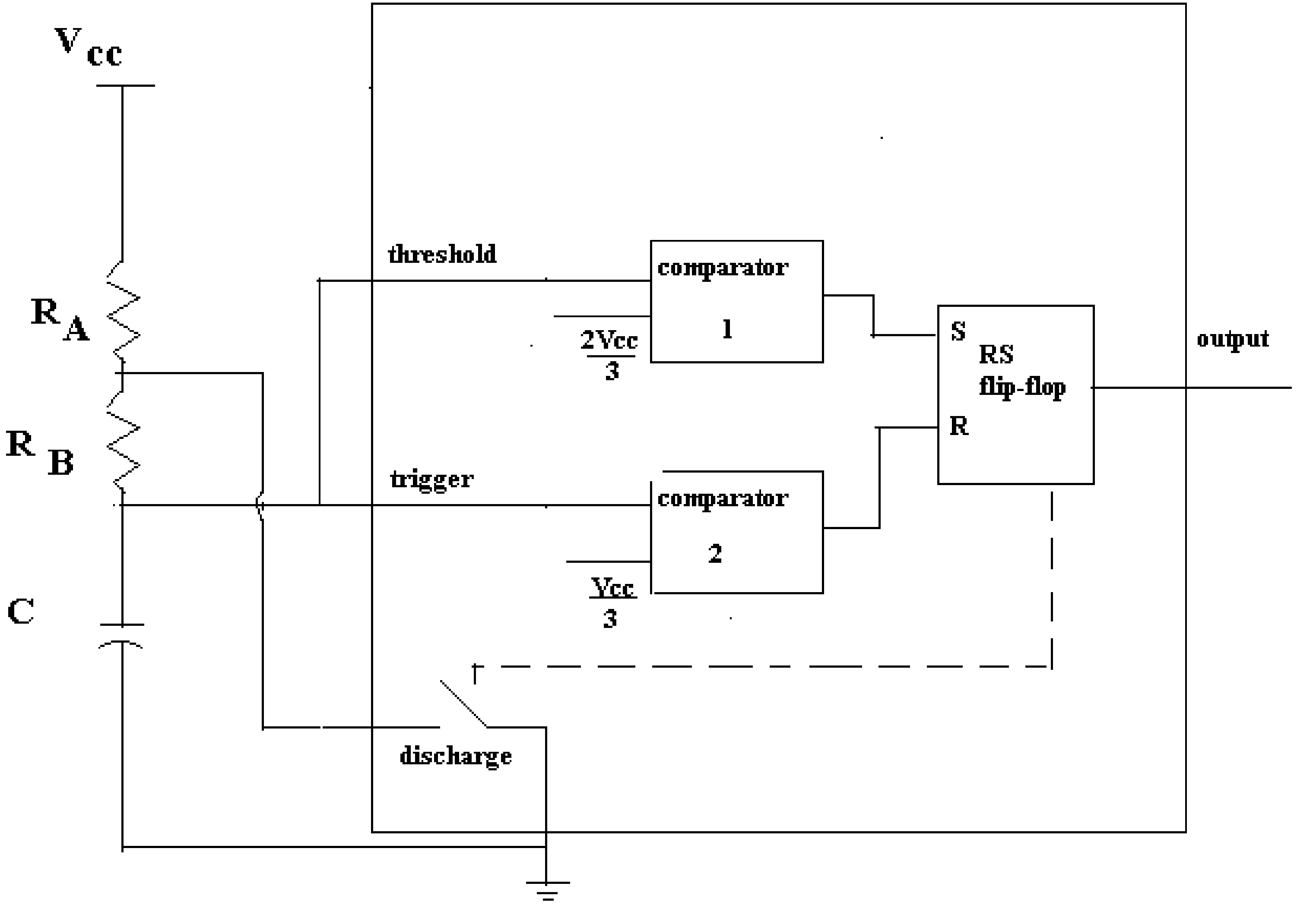
- We will measure the effect of varying frequencies on rise times, overshoot, damping, etc.
- Rules of thumb for strays—
  - Inductance ~10 nanohenries/inch
  - Capacitance– in the pfd range
- The effect of frequency—hz and mH, khz and uH, Mhz and nH have similar effects

555 Timers

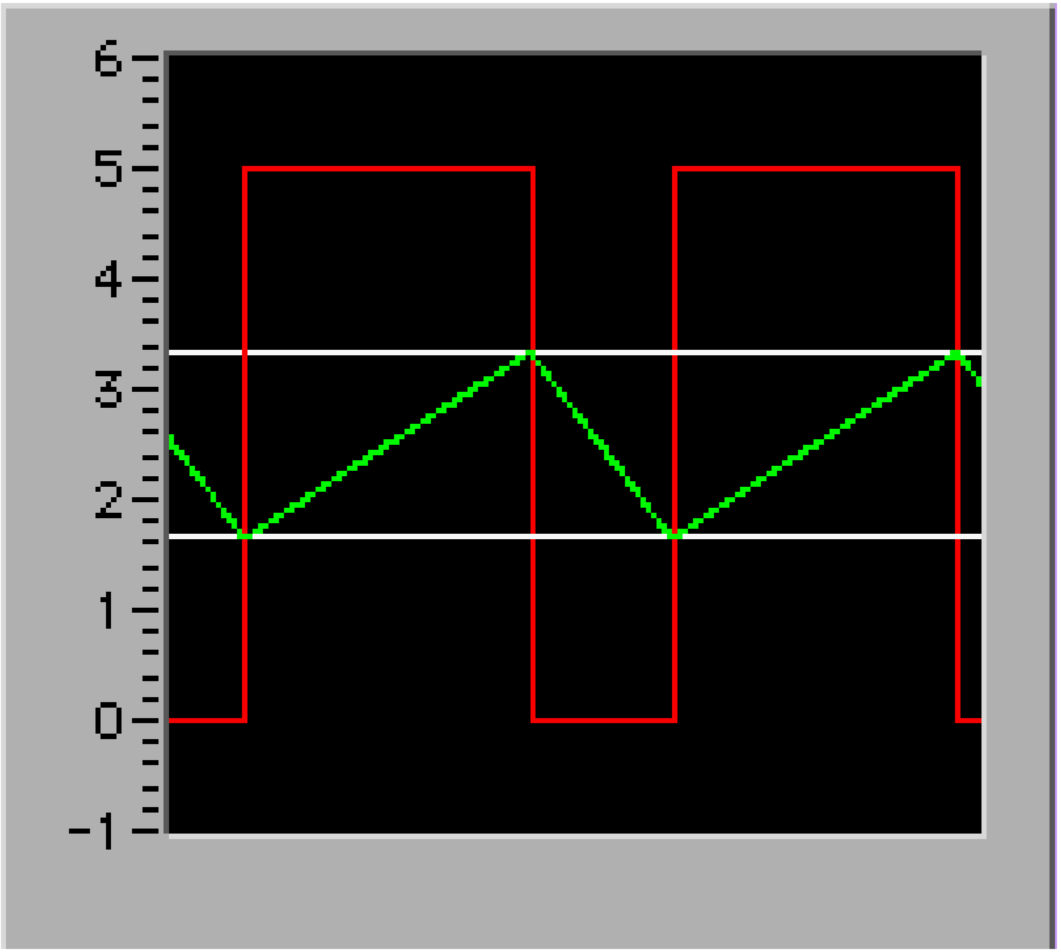
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator


Vcc
trigger
comparator
1
2Vcc
3
S
RS
flip-flop
R
output
threshold
comparator
2
Vcc
3
discharge

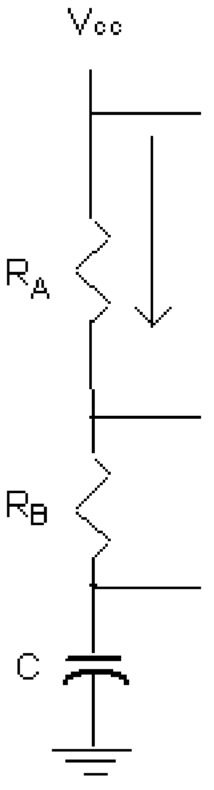
Astable mode



Cap voltage and output voltage



Capacitor charging

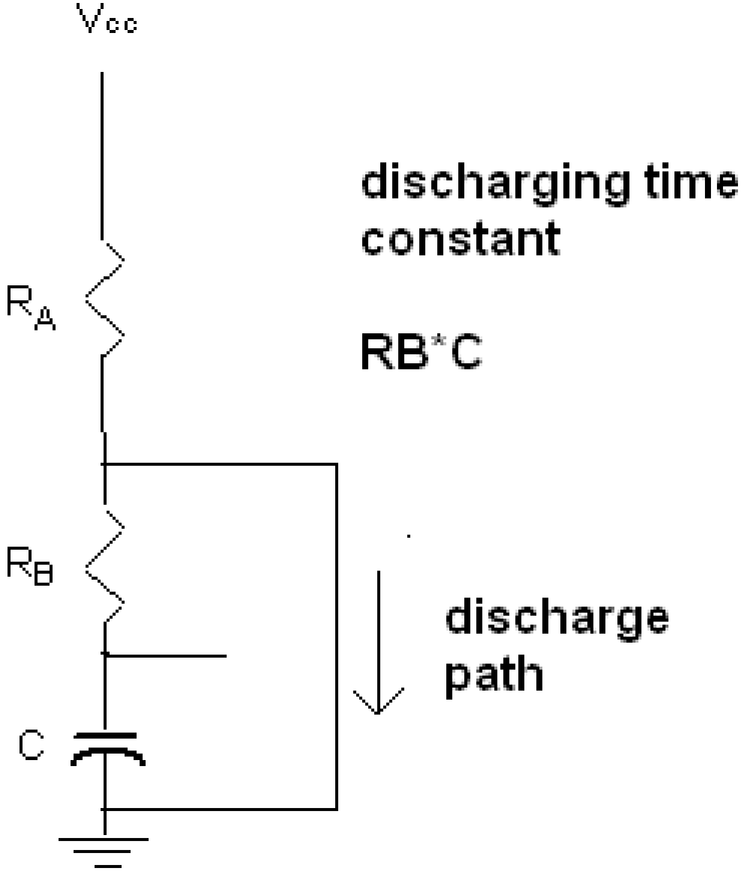


charge the diode through RA and Rb.

Time constant is

(RA+RB)*C

Capacitor Discharge



Astable mode

- Charge from Vcc/3 to 2Vcc/3–
  this takes
  $t1 = 0.693\ (RA + RB)*C$
- Discharging from 2Vcc/3 to Vcc/3
  this takes
  $t2 = 0.693\ RB*C$
- The period is T=t1+t2

Labs 10 and 11

- We will investigate the astable and monostable modes with Labview modules in Lab 10.
- We will build the astable mode in Lab 11.